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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,304	12/13/2001	Ravindra M. Kapre	01-721/LSIIP185	8043

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LSI Logic Corporation
1551 McCarthy Blvd.
M/S: D-106 Patent Department
Milpitas, CA 95035

EXAMINER
SEFER, AHMED N

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/020,304	Applicant(s) RAVINDRA ET AL	
	Examiner A. Sefer	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (claims 1-9) in Paper No. 5 is acknowledged and claims 10-21 have been cancelled.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Kusunoki US Patent No. 6,066,880.

Kusunoki discloses (see figs. 68-79, col. 3, lines 5-42 and col. 7, lines 60-65) a semiconductor device or PMOS/NMOS transistor (as in claims 6 and 7) having at least an insulating gate dielectric layer 4 and a gate fabricated upon a semiconductor substrate or p-type/ n-type (as in claims 2 and 3), a buried channel 10 or p-type /n-type buried channel (as in claims 2 and 3) implanted below the insulating gate dielectric, the buried channel being doped with a predetermined dopant so that when the gate is

biased with respect to the substrate, the buried channel is partially depleted of charge carriers, effectively increasing the thickness of the insulating gate dielectric layer.

As to claims 4 and 5, Kusunoki discloses an inversion bias from a gate to a substrate.

As to claims 8 and 9, Kusunoki discloses a MOS capacitor comprising part of a one transistor random access memory.

4. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Shigyo (JP 7-273212).

Shigyo discloses (see figs. 1-4 and abstract) a semiconductor device or PMOS/NMOS transistor (as in claims 6 and 7) having at least an insulating gate dielectric layer 15 and a gate 19 fabricated upon a semiconductor substrate or p-type/ n-type (as in claims 2 and 3), a buried channel or p-type /n-type buried channel (as in claims 2 and 3) implanted below the insulating gate dielectric, the buried channel being doped with a predetermined dopant so that when the gate is biased with respect to the substrate, the buried channel is partially depleted of charge carriers, effectively increasing the thickness of the insulating gate dielectric layer.

As to claims 4 and 5, Shigyo discloses an inversion bias from a gate to a substrate.

5. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Rotondoro US PG-Pub No. 2002/0058424.

Rotondaro discloses in fig.1 a semiconductor device having at least an insulating

gate dielectric layer 20 and a gate 30 fabricated upon a semiconductor substrate, a buried channel 80 implanted below the insulating gate dielectric, the buried channel being doped with a predetermined dopant so that when the gate is biased with respect to the substrate, the buried channel is partially depleted of charge carriers, effectively increasing the thickness of the insulating gate dielectric layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (703) 308-6601.

ANS
July 18, 2002

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800